KING FAISAL UNIVERSITY
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING

Course Code / Title: BME 310 –Bio-Electronics I **Semester / Year**: Fall /2019
Homework Assignment #: 2 **Date**: 02/10/2019 **Due Date:** 24/10/2019
Instructor: Dr. Mohammed Morsy Farag

1. Using load line analysis, determine the value of R for the circuit of Fig. P1(a) that will result in a diode current of 10 mA if E=7 V. Use the characteristics of Fig. P1(b) for the diode.

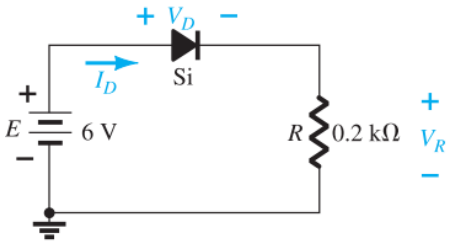


Figure1 (a)

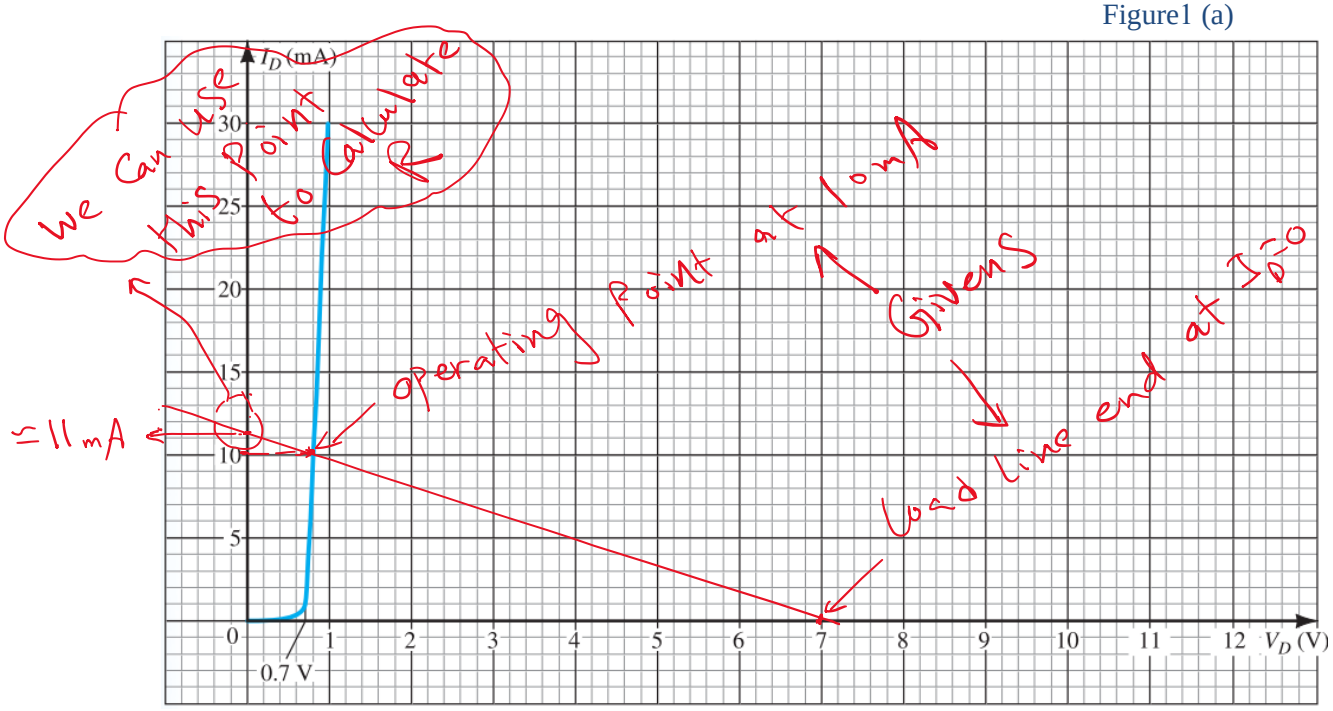
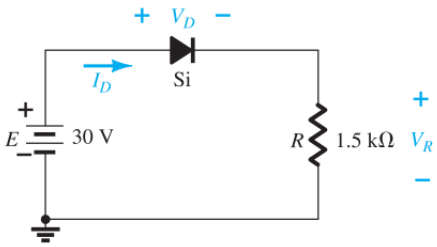


Figure 1(b)

- the load line has two ends (E, E/R).
- the givens are E=7V, and the operating point is @ I=10mA
- Plot the two points and connect them to get the load line.
- the load line intersects with I-axis at 11mA = E/R ⇒ R = 7/11 = 0.636 KΩ

2.

a. Using the approximate characteristics for the Si diode, determine V_D, I_D, and V_R for the circuit of Fig. P2.
b. Perform the same analysis as part (a) using the ideal model for the diode.
c. Do the results obtained in parts (a) and (b) suggest that the ideal model can provide a good approximation for the actual response under some conditions?



a) D is on $\rightarrow V_D = 0.7V$ (Approximate)

$\therefore V_R = E - V_D = 30 - 0.7 = 29.3\,V$

$I_D = I_R = \frac{V_R}{R} = \frac{29.3}{1.5} = 19.53\,mA$

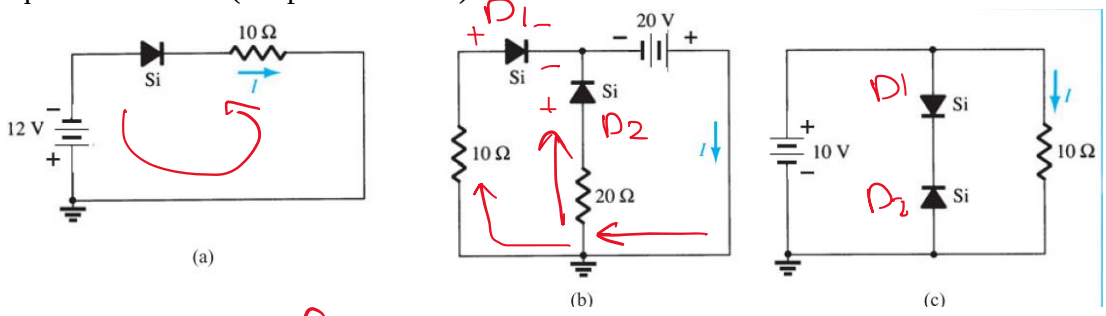
b) Ideal Model

D is on $\rightarrow V_D = 0$

$\therefore V_R = E = 30V \rightarrow I_D = \frac{30}{1.5} = 20\,mA$

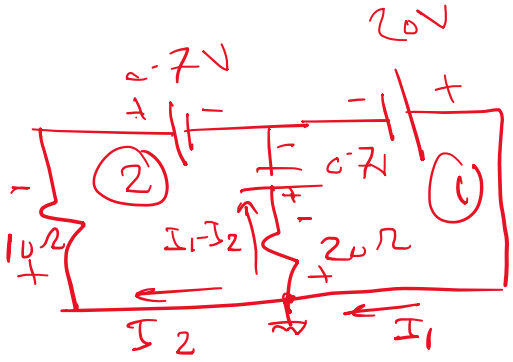
c) V_R and I_D values are very close $\rightarrow$ Ideal model is a good approximation because the supply voltage $E >> 0.7V$

3. Determine the current I for each of the diode circuits of Fig. P3 using the approximate equivalent model (simplified model) for the diode.



a) D is off $\rightarrow I = 0$

b) both D_1 & D_2 are on (Current is in the same Diode direction)



- KVL Loop (1) :-

$$20 - 20(I_1 - I_2) - 0.7 = 0$$

$$19.3 - 20(I_1 - I_2) = 0 \rightarrow (1)$$

- KVL loop (2) :-

$$0.7 + 20(I_1 - I_2) - 10I_2 - 0.7 = 0$$

$$\therefore 20(I_1 - I_2) - 10I_2 = 0 \rightarrow 20I_1 - 30I_2 = 0$$

$$\therefore I_1 = 3/2\, I_2 \rightarrow (2)$$

Sub by (2) in (1) :-

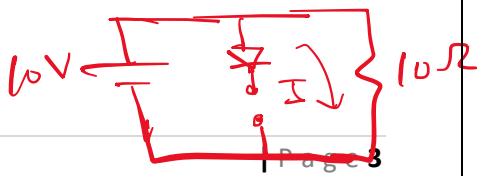
$$19.3 - 20(3/2\, I_2 - I_2) = 0$$

$$19.3 - 10I_2 = 0 \rightarrow I_2 = 1.93\ A$$

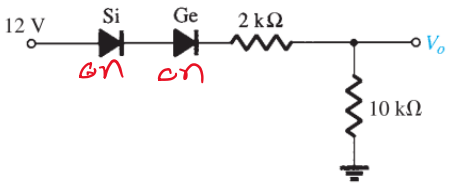
$$\therefore I_1 = 3/2\,(1.93) = 2.895\ A$$

c) D_2 is reverse-biased $\rightarrow$ O.C

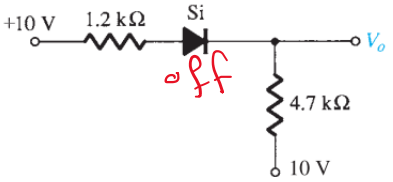
$$\therefore I = \frac{10V}{10\Omega} = 1\ A$$



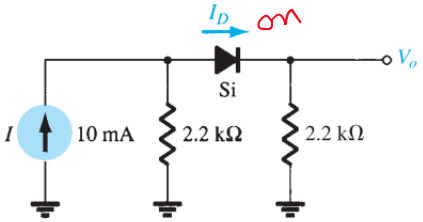
4. Determine the level of V_o for each network of Fig. P4.



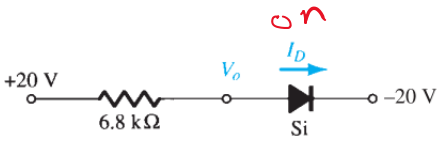
(a)



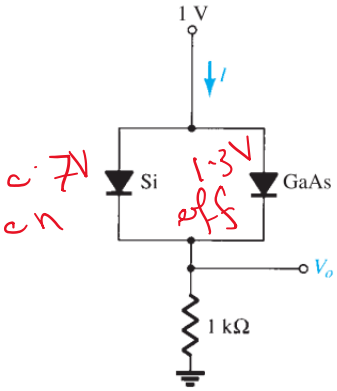
(b)



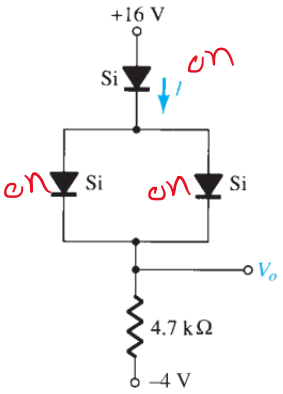
(c)



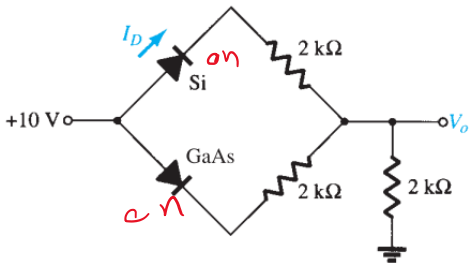
(d)



(e)



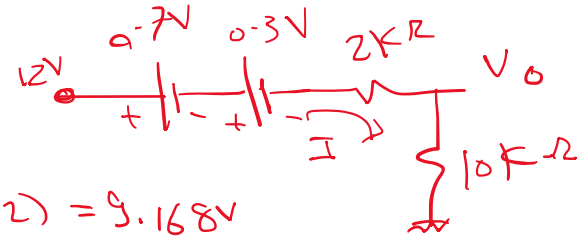
(f)



(g)

a) $I = \frac{12 - 0.7 - 0.3}{10+2} = 0.916\text{mA}$

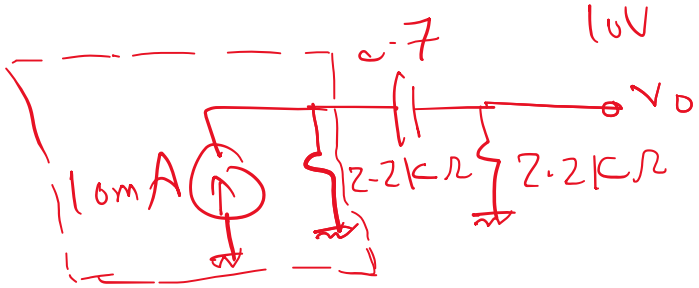
$\Rightarrow V_o = 12 - 0.7 - 0.3 - 0.916(2) = 9.168\text{V}$



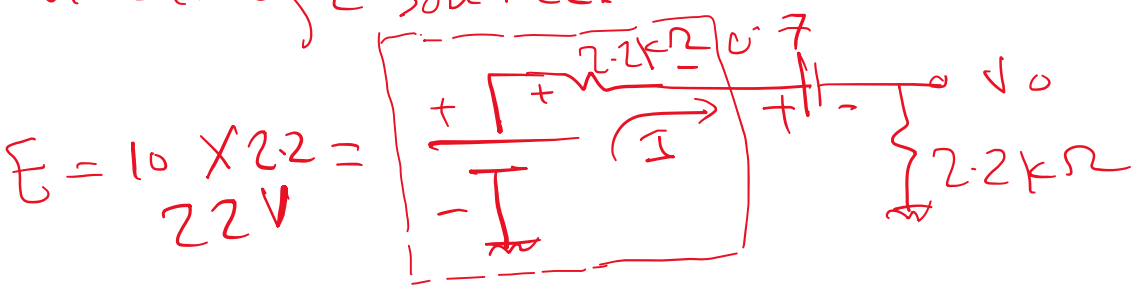
b) D is off $\longrightarrow I = 0$

$\therefore V_o = 10\text{V}$

c) D $\longrightarrow$ on



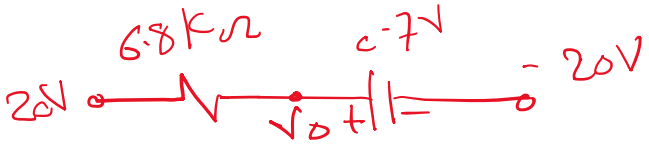
We can replace the current source by a voltage source.



$$I = \frac{22 - 0.7}{2.2 + 2.2} = 4.84\,mA$$

$$\therefore V_o = I(2.2) = 4.84(2.2) = 10.65V$$

d) Diode is on

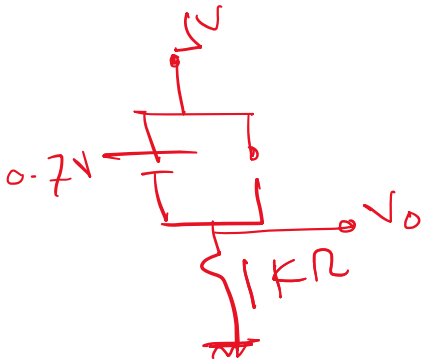


$\therefore V_o = -20 + 0.7$

$= -19.3V$

e) GaAs → off

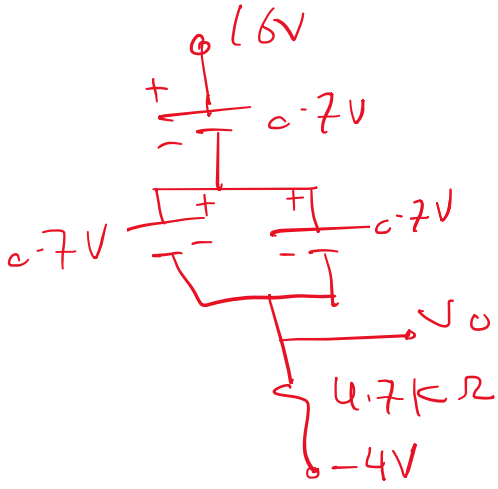
$V_o = 1 - 0.7 = 0.3V$



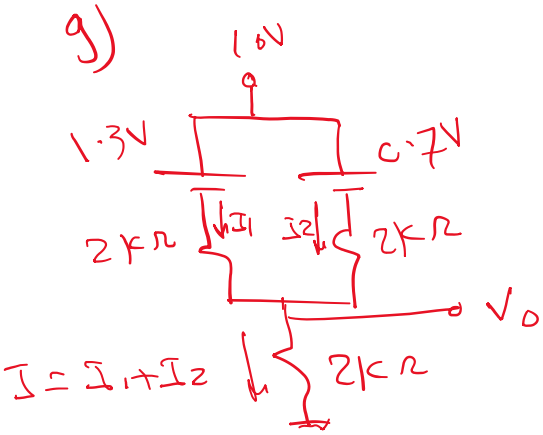
f) all Diodes are on

$V_o = 16 - 0.7 - 0.7$

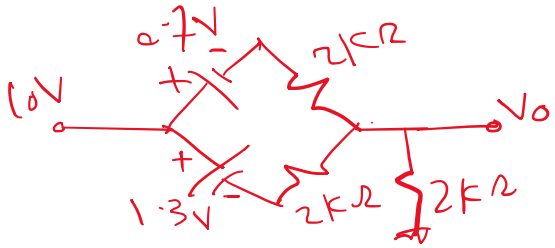
$= 14.6V$



g)



Redraw



KVL L_1 :- $10 - 1.3 - 2I_1 - 2(I_1+I_2) = 0$

$4I_1 + 2I_2 = 8.7 \longrightarrow (1)$

KVL L_2 :- $10 - 0.7 - 2I_2 - 2(I_1+I_2) = 0$

$4I_2 + 2I_1 = 9.3V \longrightarrow (2)$

from (2) $I_1 = \dfrac{9.3 - 4I_2}{2}$

sub in (1) $4\left(\dfrac{9.3-4I_2}{2}\right) + 2I_2 = 8.7$

$18.6 - 8I_2 + 2I_2 = 8.7$

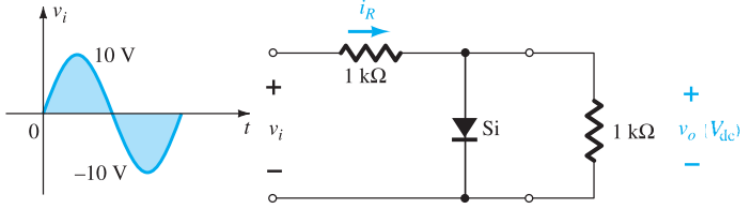
$\Rightarrow I_2 = \dfrac{18.6-8.7}{6} = 1.65\,mA$

$\therefore I_1 = \dfrac{9.3 - 4(1.65)}{2} = 1.35mA$

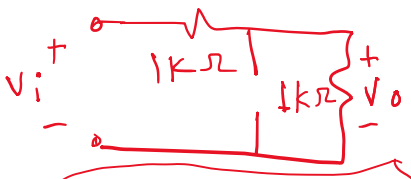
$\therefore V_o = 2(1.35 + 1.65) = 6\,V$

5. For the network of Fig. P6, sketch v_o, i_r and determine V_{dc}.

this is a half-wave rectifier circuit



-when D is off (o.c):



$V_o = \dfrac{1}{1+1} V_i = V_i/2$

for D-off :-

$V_o < 0.7$

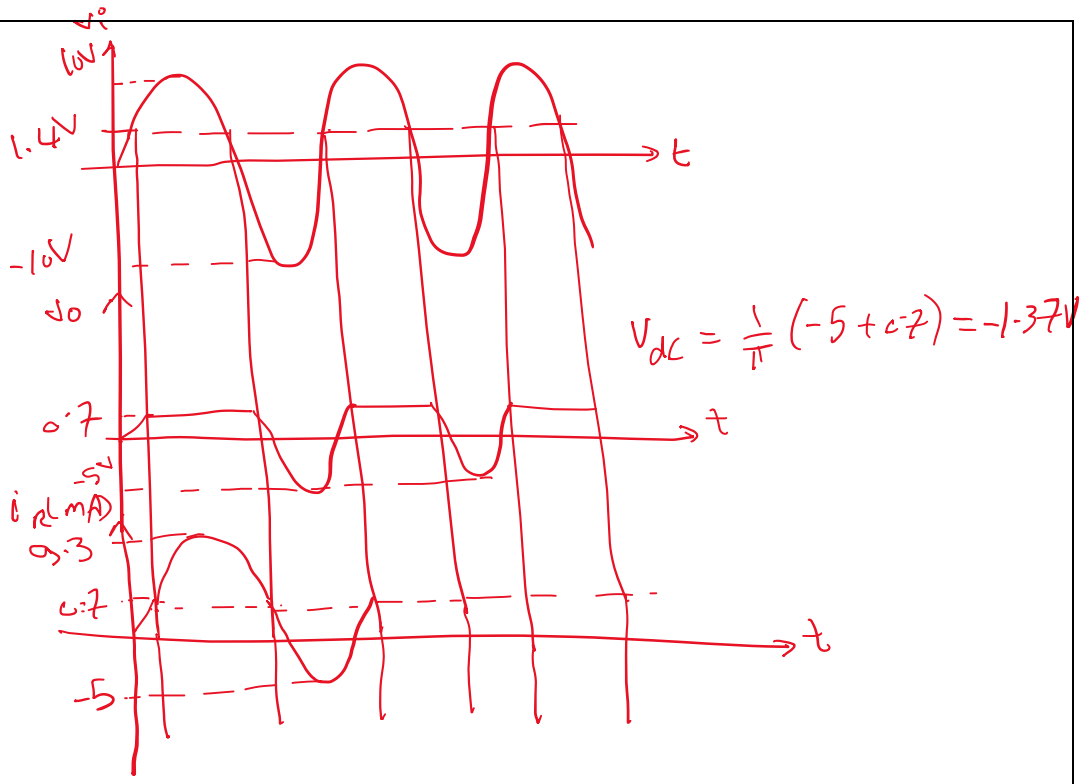
$\Rightarrow V_i/2 < 0.7 \Rightarrow V_i < 1.4V$

$\therefore$ for D-on $\Rightarrow V_i \geq 1.4V$

when D-on

$\Rightarrow V_o = 0.7V$

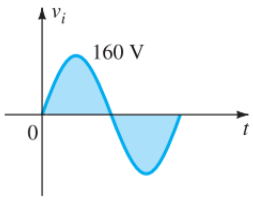
$i_R = \dfrac{V_i - V_o}{1k\Omega} = (V_i - V_o)\,mA$

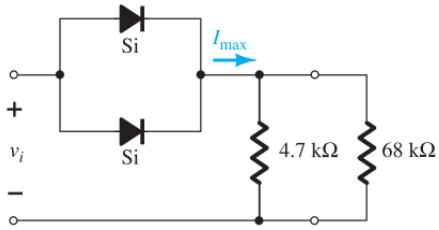


6.

a. Given P_{max}=14 mW for each diode at Fig. P6, determine the maximum current rating of each diode (using the approximate equivalent model).
b. Determine I_{max} for the parallel diodes.
c. Determine the current through each diode at $V_{i_{max}}$ using the results of part (b).
d. If only one diode were present, what would be the expected result?

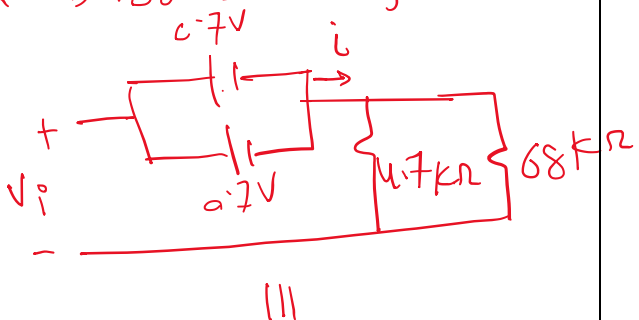
a) $P_{max} = 14mW$
(for Silicon Diode)
$V_{D_{on}} = 0.7V$





for any element $P = VI$
for the Diode: $P_{max} = V_{D_{on}} I_{max}$
$\therefore 14 = 0.7 I_{max} \Rightarrow I_{D_{max_rated}} \simeq 20mA$

b) for the parallel Diodes:
if $V_i > 0.7$ ⟶ both Diodes are forward

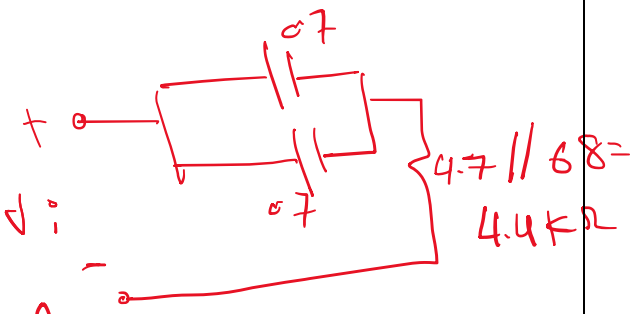


$i = \frac{V_i - 0.7}{4.4}$

III

For $V_i = V_{i,max} = 160V$

$i_{max} = \frac{160 - 0.7}{4.4} = 36.2mA$



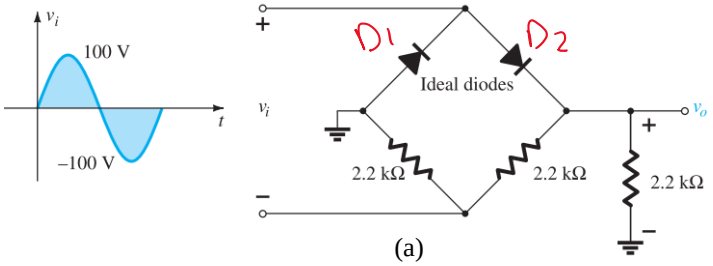
c) $i_{(Diode)} = \frac{i_{max}}{2} = \frac{36.2}{2} = 18.1mA$

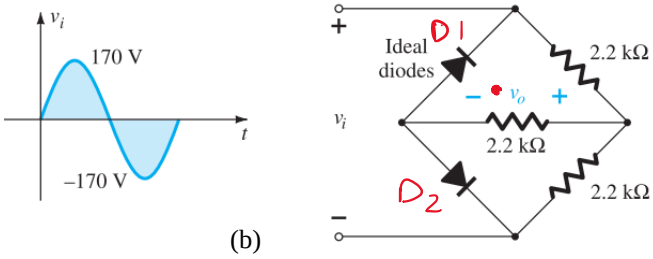
d) $i_{Diode} < i_{Dmax_rated}$ $(18.1mA < 20mA)$

* if only a Single Diode exists → $i_{Diode} = 36.2mA$

∴ $i_D > i_{D_{max_rated}}$ → Diode will be burned.

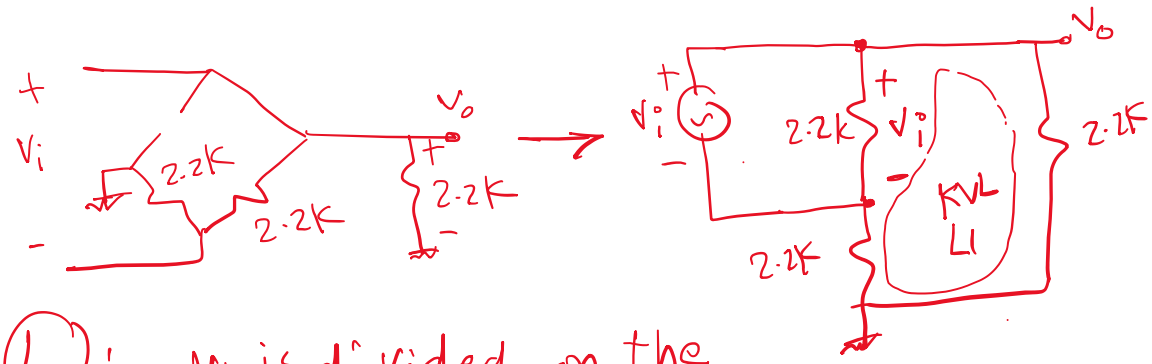
7. Sketch v_o for the following networks of Fig. P7 and determine the dc voltage available.





a)

① $V_i > 0$ → D_1 → off, D_2 → on

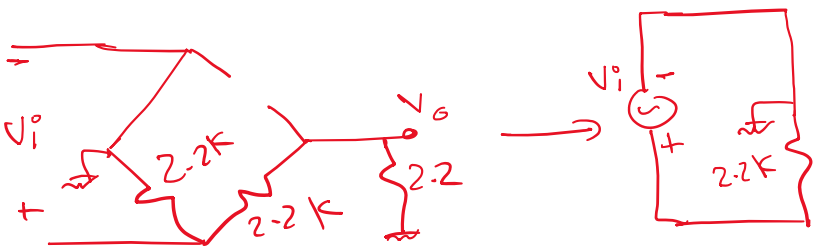


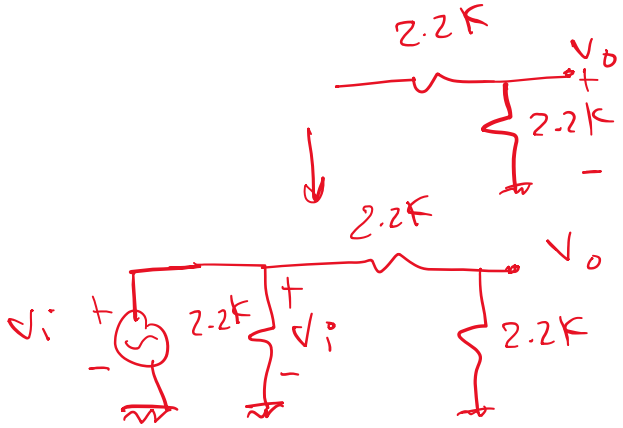
KVL (L1) :- V_i is divided on the equal Resistors (2.2kΩ) → Each resistor will get $V_i/2$

∴ for $V_i > 0$ → $V_o = V_i/2$

② for $V_i < 0$

D_1 → on, D_2 → off





Similar to (1)

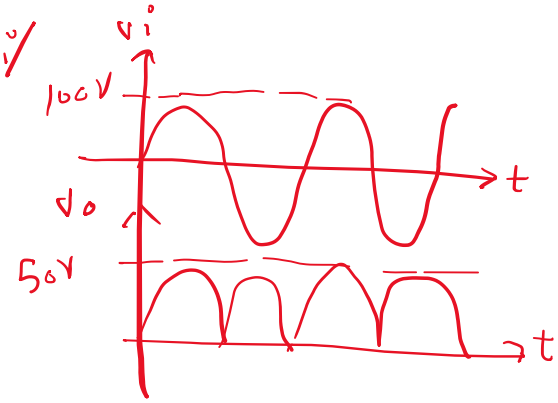
V_i is divided on the two 2.2KΩ resistors.

$\Rightarrow$ Each resistor gets $V_i/2$.

V_i has negative value while V_o has +ve value.

$\Rightarrow V_o = -V_i/2$

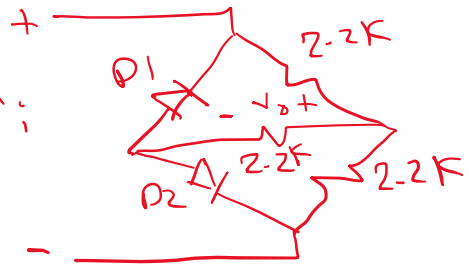
Sketch V_o vs V_i

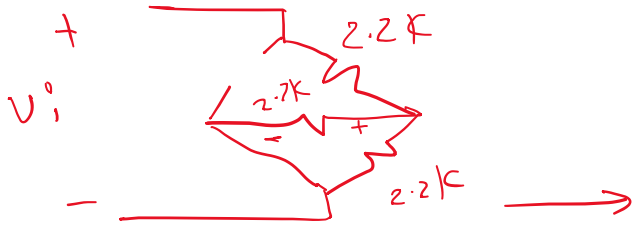


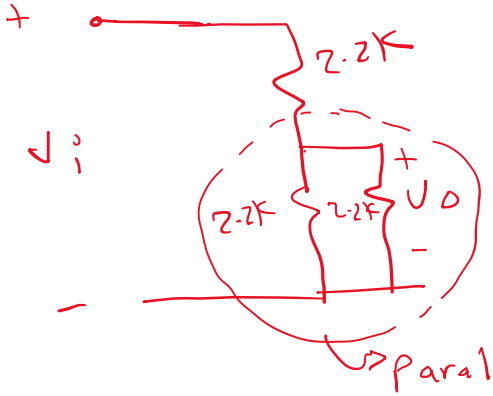
full-wave rectified output

(b)

(1) $V_i > 0 \rightarrow$ D_1 - off, D_2 - on





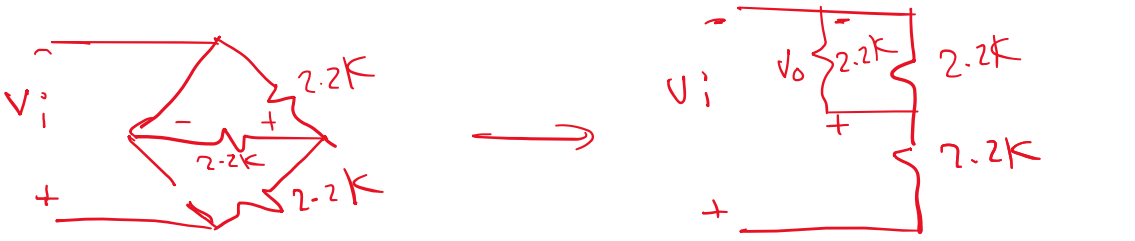


$$V_o = V_i \cdot \frac{2.2 \,//\, 2.2}{2.2 + 2.2 \,//\, 2.2}$$

$$= V_i \frac{1.1}{2.2 + 1.1} = V_i/3$$

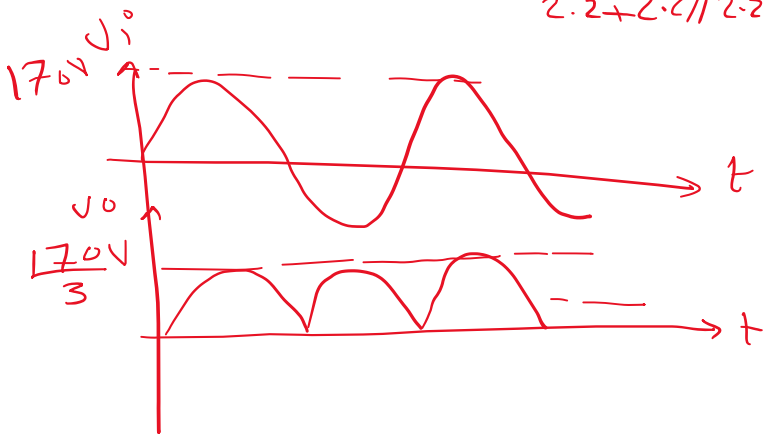
(2) $V_i < 0$

D_1 - on, D_2 - off

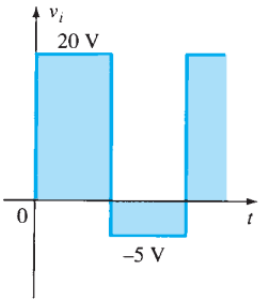


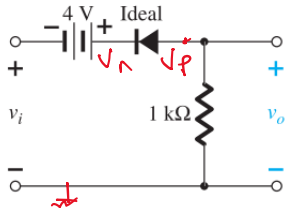
Similar to (1) : $V_o = -V_i \dfrac{2.2 \parallel 2.2}{2.2 + 2.2 \parallel 2.2} = -V_i/3$

Sketch/

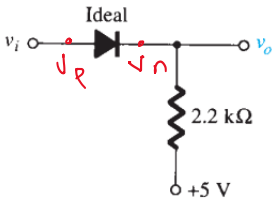


8. Sketch v_o for each network of Fig. P8 for the inputs shown.

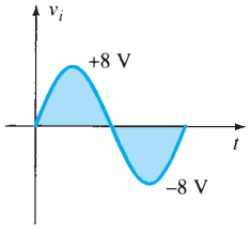


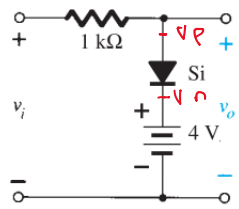


(a)

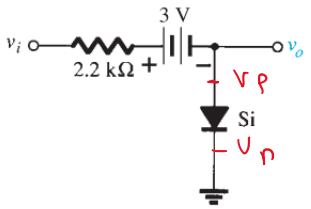


(b)





(a)



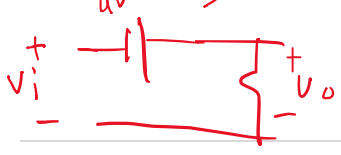
(b)

(a) for D-off /

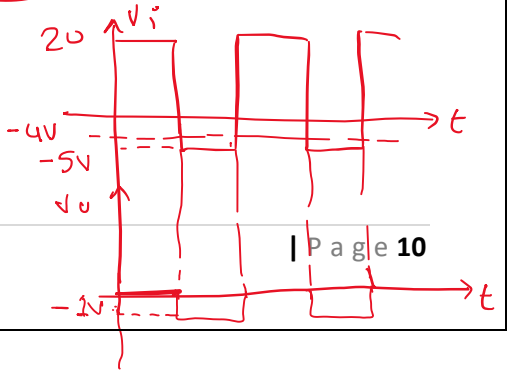
$V_p = 0$, $V_n = V_i + 4 \rightarrow V_D = (-V_i - 4V < 0) \rightarrow$ for D-off

$\therefore V_i \geq -4V \rightarrow V_o = 0$

D-on $\rightarrow V_i < -4V \rightarrow V_o = V_i + 4$



$\therefore V_o = -5 + 4 = -1V$



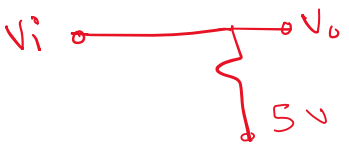
(b) for D-off / $V_p = V_i$, $V_n = 0 \rightarrow V_D = V_i$

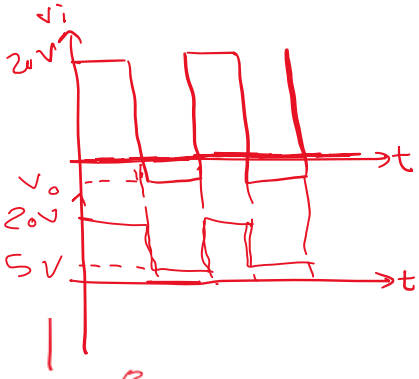
$\therefore V_D < 0 \rightarrow V_i < 0 \rightarrow$ D-off

$\therefore$ for $V_i < 0 \rightarrow V_o = +5V$

for D-on $V_i > 0$

$\rightarrow V_o = V_i$



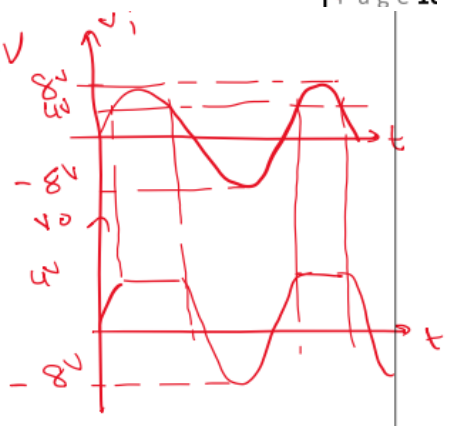


(c) for D-off : $V_p = V_i$, $V_n = 4V$

$\Rightarrow V_D = V_i - 4V < 0 \Rightarrow V_i < 4V$

$\therefore V_o = V_i$

for D-on $\rightarrow V_i \geq 4V \Rightarrow V_o = 4V$



(a) for D-off :-

$V_p = V_i - 3V$

$V_n = 0$

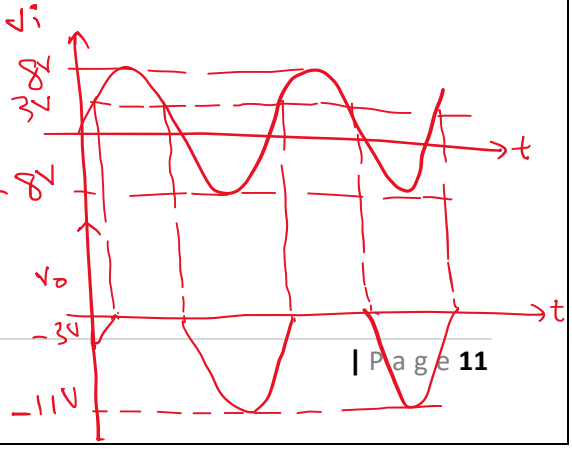
$\therefore V_D = V_i - 3V < 0$

$\therefore V_i < 3V \rightarrow$ D-off

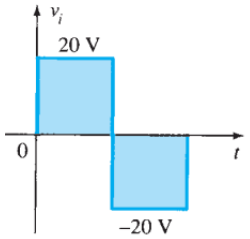
$\therefore V_o = V_i - 3V$

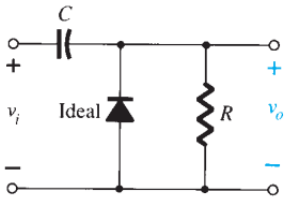
for $V_i \geq 3V \rightarrow$ D-on :

$\therefore V_o = 0$

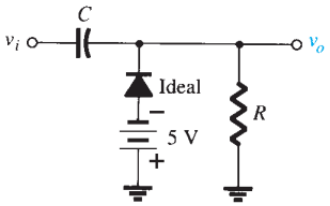


9. Sketch v_o for each network of Fig. P9 for the inputs shown.

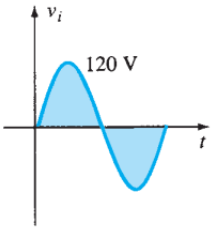


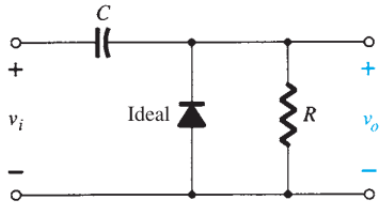


(a)

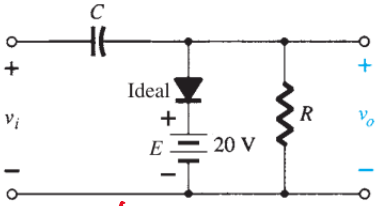


(b)





(a)



(b)

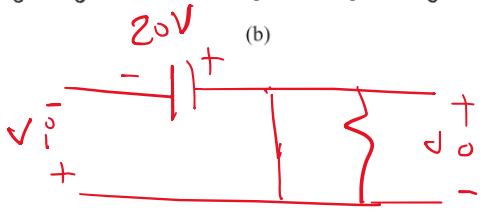
(a) for $V_i < 0$ → D-on

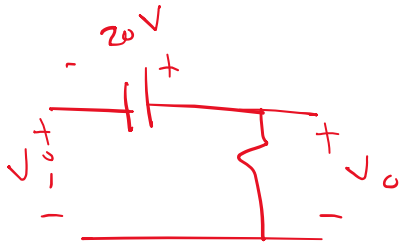
→ C charges to V_m

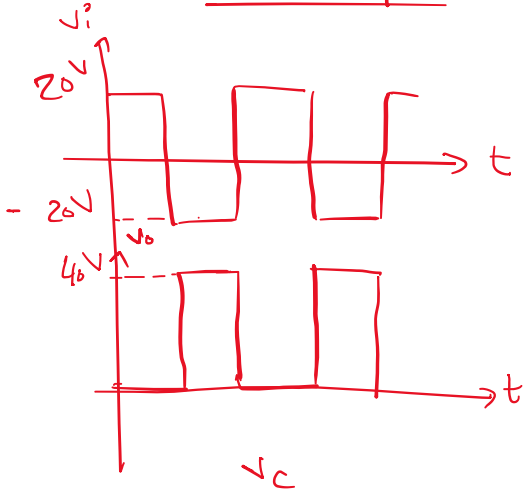
$\therefore V_o = 0$

then C keeps its charge and D is turned off.

$\therefore V_o = V_i + 20V$







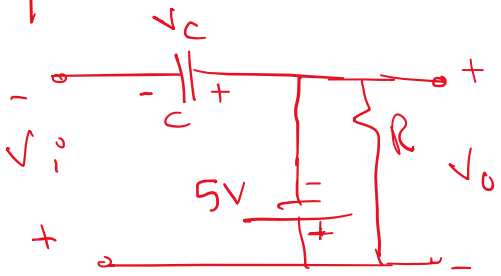
(b) when $V_i < 0$ → D-on

$V_C = V_i + 5V$

the Capacitor charges

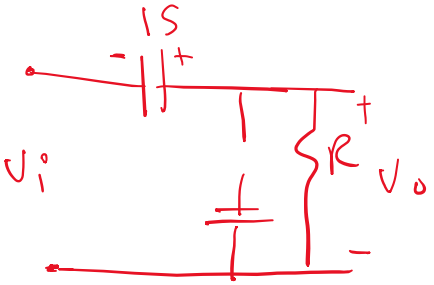
to $V_C = 20 - 5V = 15V$

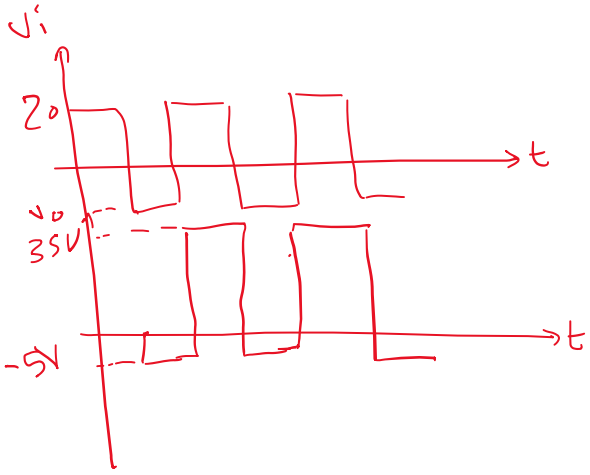
$V_o = -5V$



then, the Diode turns off and the Capacitor holds its Charge.

$\therefore V_o = V_i + 15$





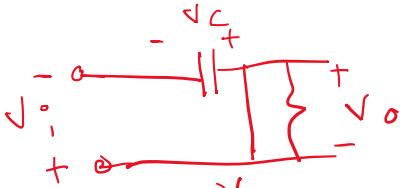
c) when $V_i < 0 \rightarrow$ D-on

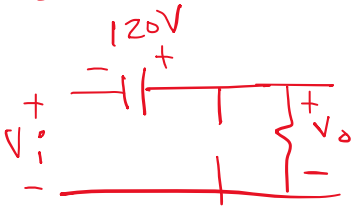
the Capacitor Charges:

$V_C = V_m = 120V$, $V_o = 0$

Then D will be of off

$\therefore V_o = V_i + 120V$





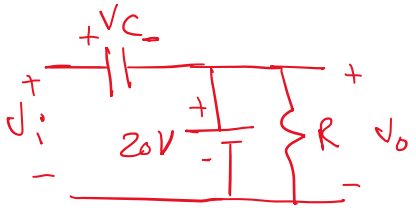
(d) when $V_i > 20V$

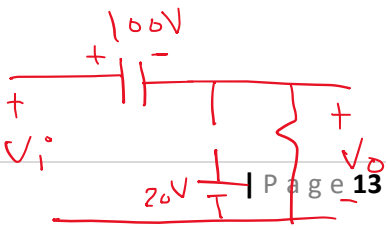
$\rightarrow$ D-on $\rightarrow V_o = 20V$

the Capacitor charges to V_m

$\therefore V_C = V_i - 20 = 120 - 20V = 100V$

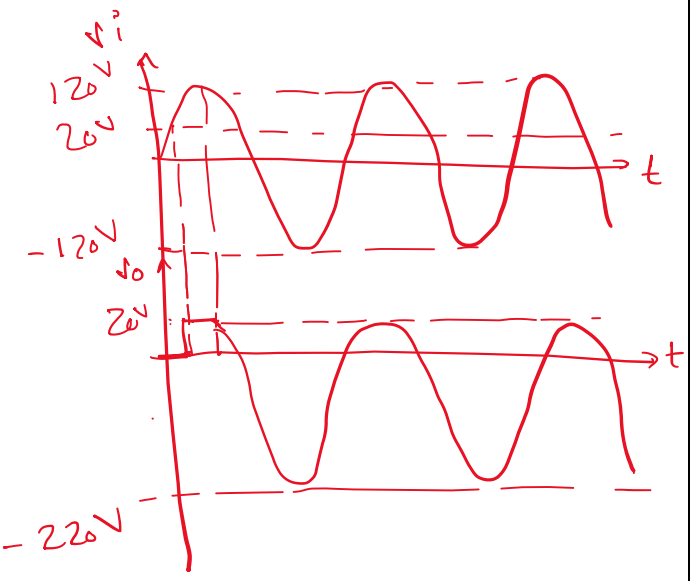
Then the Diode is off and Ids



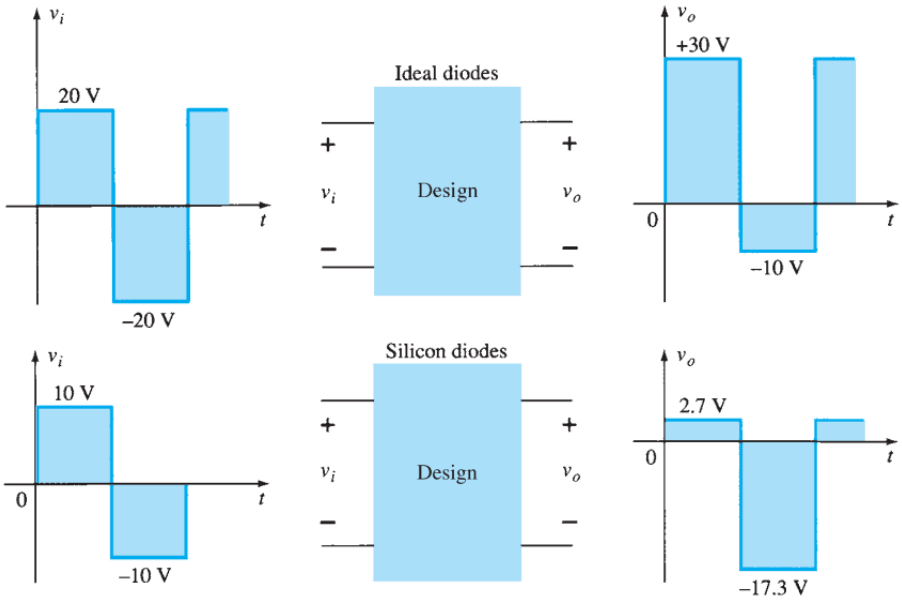


the Capacitor has its charge

$\therefore V_o = V_i - 100$

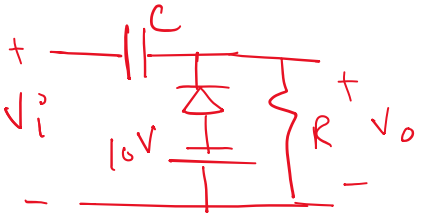


10. Design clamper circuits to perform the functions indicated in Fig. P10.

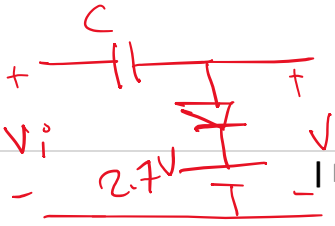


By checking the Clampers Summary table (slide 80)

a) the clamper circuit is :-

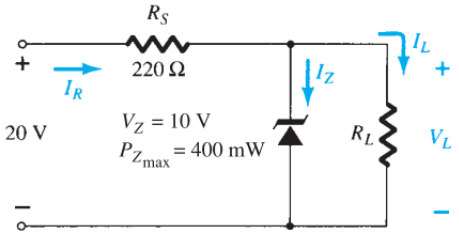


b) the Clamper Circuit is :-

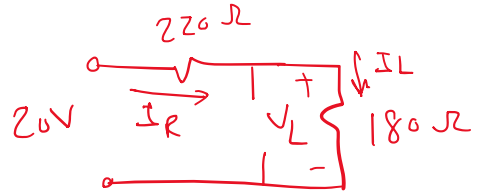


11.

a. Determine V_L, I_L, I_Z, and I_R for the network of Fig. P11 if R_L= 180Ω.
b. Repeat part (a) if R_L= 470Ω.
c. Determine the value of R_L that will establish maximum power conditions for the Zener diode.
d. Determine the minimum value of R_L to ensure that the Zener diode is in the "on" state.



a) $R_L = 180\Omega$



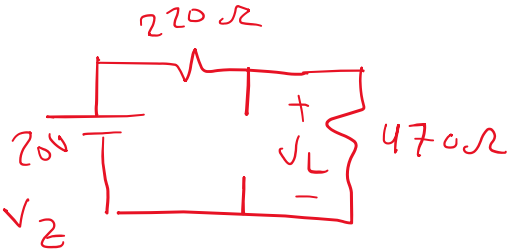
Assume $D_Z \rightarrow$ off (o.c)

$V_L = \frac{180}{180+220}(20) = 9\,V < V_Z$ (Assumption is true)

$\therefore I_R = I_L = \frac{20}{180+220} = 50\,mA$, $I_Z = 0$

$\therefore V_R = V_i - V_L = 20 - 9 = 11\,V$

b) $R_L = 470\Omega$

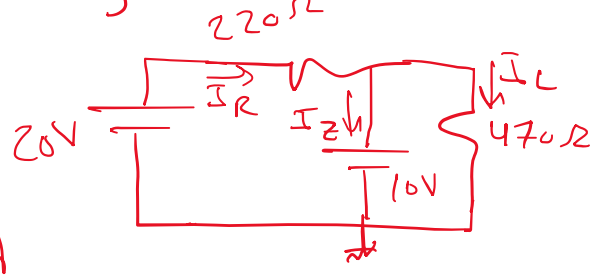


Assume D_Z - off (o.c)

$V_L = 20\,\frac{470}{470+220} = 13.6\,V > V_Z$

$\therefore$ Assumption is wrong and D_Z is in the Zener region.

- Redraw the Ckt:-



$I_L = \frac{10}{470} = 21.3\,mA$

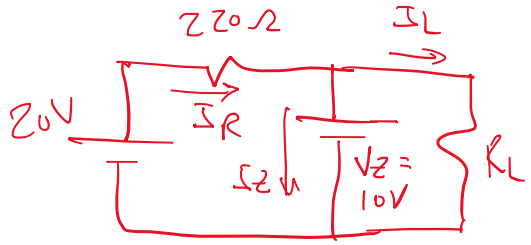
$I_R = \frac{20-10}{220} = 45.45\,mA$

$\therefore I_Z = I_R - I_L = 45.45 - 21.3 = 24.15\,mA$

$\therefore P_Z = I_Z V_Z = 24.15\,(10) = 241.5\,mW$

c) $R_L = ??$ for P_{zm}

D_z is on



$P_{zm} = 400mW = V_Z I_Z$

$\therefore I_{Zm} = \frac{400mW}{10V} = 40mA$

$I_R = \frac{20-10}{220} = 45.45mA$

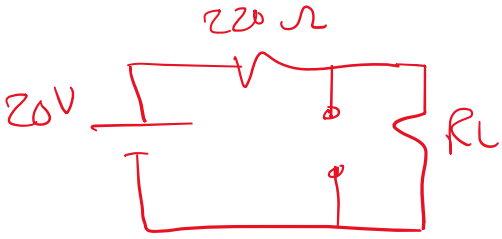
$\therefore I_L = I_R - I_{Zm} = 45.45 - 40 = 5.45mA$

$\therefore R_{Lmax} = V_L / I_L = \frac{10}{5.45} = 1835\Omega = 1.835K\Omega$

d) $R_{Lmin} = ??$ to ensure D_z is in the Zener region.

Assum D_z is off

$V_L = \frac{R_L}{R_L + 220}(20)$



to make D_z works in the zener region :-

$V_L \geq V_Z \Rightarrow \frac{R_L}{R_L+220}(20) \geq 10$

$\therefore \frac{R_L}{R_L+220} \geq 1/2 \Rightarrow R_L \geq \frac{1}{2}R_L + 110$

$\therefore R_L \geq 220\Omega$

$\therefore R_{Lmin} = 220\Omega$ (to ensure D_z is on)